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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,156	07/06/2001	Nagahisa Watanabe	210854US2S	2834

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,156	WATANABE, NAGAHISA	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-16* is/are pending in the application.

4a) Of the above claim(s) *7-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Marked up figure* .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 5, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgess, US Patent No. 4,642,160 in view of Gorrell et al., US Patent No. 5,747,358.

Regarding claim 1, Burgess discloses a printed wiring board, comprising:

an insulating layer having a first surface and a second surface located on an opposite side of said first surface; a plurality of circuit patterns formed by etching metal foils laminated on at least said first surface and said second surface of said insulating layer (printed circuit board with wiring layer on top and bottom surface of the insulating layers, see figure 9);

a via formed on said insulating layer, said via having one end opened on said first surface of said insulating layer and other end closed by a circuit pattern of said plurality of circuit patterns formed on a part of said insulating layer other than said first surface (via 40 open at one end and the other end is closed by internal wiring layer, see figure 9);

a first plating layer having a first portion that covers an inner surface of said via and a circuit pattern of said plurality of said circuit patterns that closes said other end of said via and which is exposed within said via, and a second portion that covers a circuit pattern of said plurality of circuit patterns that is on said first surface and which continues to said one end of said via; and (plating layer 38 conductor run 40, see figure 8 and 9); except

a second plating layer laminated on said first plating layer and electrically connecting a circuit pattern of said plurality of circuit patterns formed on said first surface with said circuit pattern of the plurality of circuit patterns that closes said other end of said. However applying a second plating layer is known in the art for getting the desired thickness of the conductive material or to coat the via, pad and patterns with noble metal to have better electrical connection and also to protect from the environmental corrosion. Also, it is known in the art to provide a very thin plating layer in the via hole along with the board surface, and apply a subsequent plating layer on the desired area along with the via hole. Gorrell discloses such additional plating, see Gorrell, via 40, figure 16, column 7, line 54 to column 8, line15. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide circuit board of Burgess with a second plating layer as taught by Gorrell in order to get the desired thickness and / or protection from the environmental corrosion.

Regarding claim 2, the modified circuit board of Burgess further discloses both the first and second plating layer. The first plating can be considered a ground work depending upon its use. If it is a plating for having a conductive surface on the nonconductive via, it can be a ground work for subsequent plating.

Regarding claim 5, the modified circuit board of Burgess further discloses the insulating layer and said plurality of circuit patterns form a laminate, and one of said plurality of circuit patterns is formed inside insulating layer, is exposed with in said via, and covered by said first plating layer, see figure 9.

Regarding claim 14, the modified circuit board of Burgess further discloses the second portion of said first plating layer is a flange portion having a shape that project over the circuit pattern formed on said one end of said via, see figure 9.

Regarding claim 15, the modified circuit board of Burgess further discloses the second plating layer has a flange portion laminated on said flange portion of said first plating layer as applied to claim 1 above.

Regarding claim 16, the modified circuit board of Burgess further discloses the increased thickness outside the via openings in the flange area as applied to claim 1 and 15 above.

Response to Arguments

2. Applicant's arguments filed November 14, 2002 have been fully considered but they are not persuasive.

(I). Thickness of the circuit pattern:

the applicant's argument about the thickness of the pattern is considered, but not found persuasive. Nothing is claimed for the increase or decrease of the pattern. Further, during plating, the area where no increase in the thickness is required can be shielded by plating resist and the area where thickness is to be to be increased will in the subsequent plating will be kept exposed.

(II) the argument about the secondary prior art, of Gorrell not disclosing the connection between the circuit patterns is considered in but not found persuasive. First, the secondary prior art was used as a support to disclose that patterns with second plating layer is known in the art and a person with ordinary skill in the art will be able to use which is known in the art for getting the desired results, such as to increase the thickness or to provide a protective layer or to provide a layer with better connection property to be connected with other circuit board. Second, a red marked copy of figure 16 of Gorrel is attached for further clarification of connection of two patterns with via holes.

Conclusion

3. **THIS ACTION IS MADE FINAL.**

New explanation is given because of the amendment / addition of the new claims.

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chang et al., discloses a distribution structure with a thin electro plating layer on the bottom surface and via hole with final plating of copper and gold, see column 4, line 15-40, figure 3-5, similar to the present invention.

Rokugawa et al., discloses blind via for connecting a circuit pattern on one side with that on the other side, and use of seed layer for providing the subsequent plating layer.

Blackwell et al., discloses a thin film substrate with a seed layer having via for connecting the pattern on one side of the substrate with that on the other side.

Foster et al., discloses a flexible circuit with blind via.

Bhatt et al., discloses use of seed layer for providing additional metal plating layer.

Uzoh et al., discloes use of seed layer for providing electro plated lead–tin or other terminal metallurgies.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ibp
January 15, 2003

Appl # 09/899,156
GAU: 2827

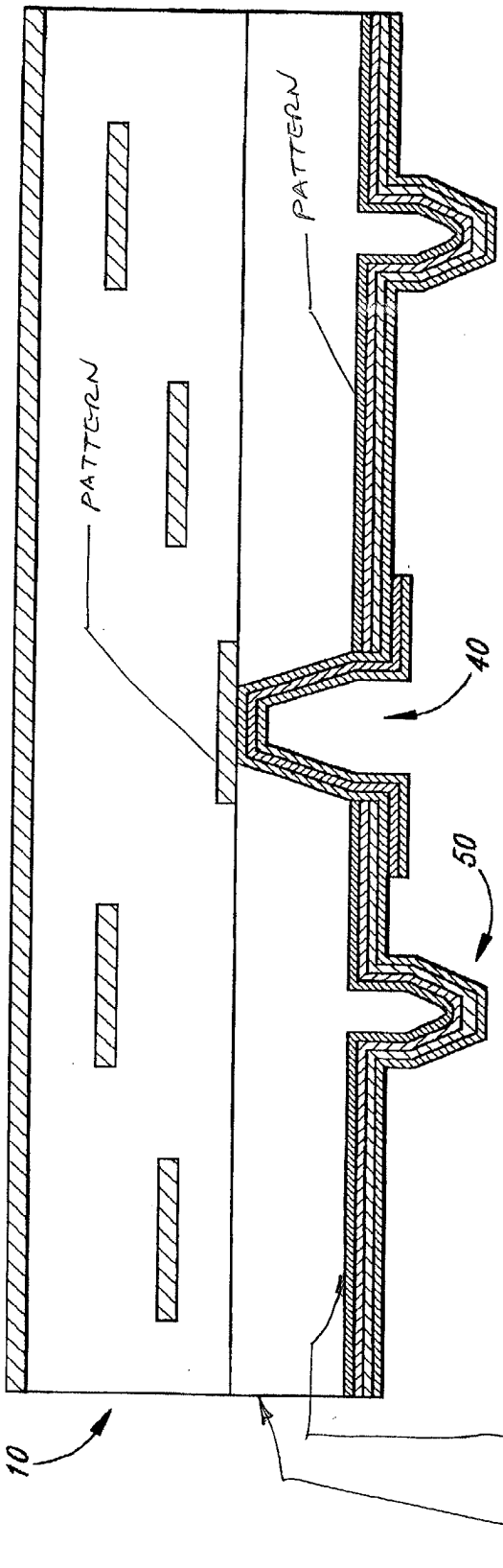

Fig. 16